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Application Number	09/759,557
Filing Date	01-12-2001
First Named Inventor	John Lee Barry
Title	Algorithmic Test Pattern Generator, with Built-In-Self-Test (BIST) Capabilities, for Functional Testing of a Circuit
Art Unit	2133
Examiner Name	TORRES, Joseph D.
Attorney Docket Number	

I hereby revoke all previous powers of attorney given in the above-identified application.

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Statement under 37 CFR 3.73(b) (Form PTO/SB96) submitted

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SIGNATURE of Applicant or Assignee of Record

Signature /Bart T. Thomas/ Date 2013-03-21  
Name Bart T. Thomas Telephone 214-479-1255  
Title and Company Vice President and Secretary, National Semiconductor Corporation

**NOTE:** Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.

\*Total of 1 form is submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (or by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, PO Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO** **Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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**STATEMENT UNDER 37 CFR 3.73(b)**Applicant/Patent Owner: National Semiconductor CorporationApplication No./Patent No.: 09/759,557 Filed/Issue Date: 01-12-2001Entitled: Algorithmic Test Pattern Generator, with Built-In-Self-Test (BIST) Capabilities, for Functional Testing of a Circuit

National Semiconductor Corporation, a Corporation  
 (Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

- the assignee of the entire right, title, and interest; or
- an assignee of less than the entire right, title and interest.

The extent (by percentage) of its ownership interest is    %

In the patent application/patent identified above by virtue of either.

A. [X] An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 016382, Frame 0648, or for which a copy thereof is attached.**OR**

B. [ ] A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as shown below:

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[ ] Additional documents in the chain of title are listed on a supplemental sheet.

[ ] Copies of assignments or other documents in the chain of title are attached.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, if the assignment is to be recorded in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Bart T. Thomas/

Signature

2013-03-21

Date

Bart T. Thomas

Printed or Typed Name

214-479-1255

Telephone Number

Vice President and Secretary, National Semiconductor Corporation

Title